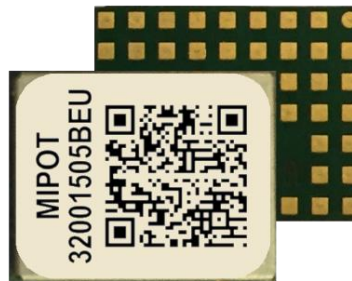


Wireless Protocol Modules MiP Series

32001505xEU Family

Host Based LoRa™ Module

Datasheet



Overview

The 32001505xEU is a family transceivers operating in the 868 MHz SRD Band optimized for very long range, low power applications, suitable for LPWA networks. Based on LoRa® RF Technology and LoRaWAN™ protocol, it provides ultra-long range spread spectrum communication and high interference immunity.

Thanks to its small LGA form factor (11.3 mm x 8.9 mm) and its low current consumption, this module allows the implementation of highly integrated low power solutions for Internet of Things (IoT) applications, security systems, sensor networks, metering, smart buildings, agriculture, and supply chain management.

The available radio stacks support a wide range of applications using the LoRa modulation, accelerating the development of a LoRaWAN application (32001505BEU), or a local star network using the LoRa Mipot stack (32001505CEU). Using the LoRa Modem stack (32001505DEU), it is easy to create point-to-point applications or build a more complex custom stack. The 32001505FEU contains all the aforementioned stack allowing to switch between them at runtime.

Contents

1. Product Features	3
2. Mechanical Dimensions	4
3. Pin Definition	5
4. Hardware Integration	7
4.1. Decoupling capacitors	7
4.2. Layout guidelines.....	7
5. Electrical Characteristics	7
5.1. Absolute Maximum Ratings.....	7
6. Operating Condition	8
GENERAL ELECTRICAL CHARACTERISTICS @ 25 °C	8
RECEIVER ELECTRICAL CHARACTERISTICS @ 25 °C	8
TRANSMITTER ELECTRICAL CHARACTERISTICS @ 25 °C	9
7. Temperature Range Curves	10
8. Safety note	10
9. Application Notes	11
10. Ordering Information	11
11. Regulatory Approvals	11
12. Revision History	12

1. Product Features

Mechanical highlights:

- ✓ Extremely compact dimensions
- ✓ LGA pattern

Low power characteristics:

- ✓ Sleep current consumption 2.2 μ A
- ✓ 11 mA in RX mode

RF performances:

- ✓ -135 dBm Sensitivity @LoRa®
- ✓ +14 dBm Output Power

Additional features:

- ✓ Smart serial interface selector (UART, LPUART, SPI, I²C)

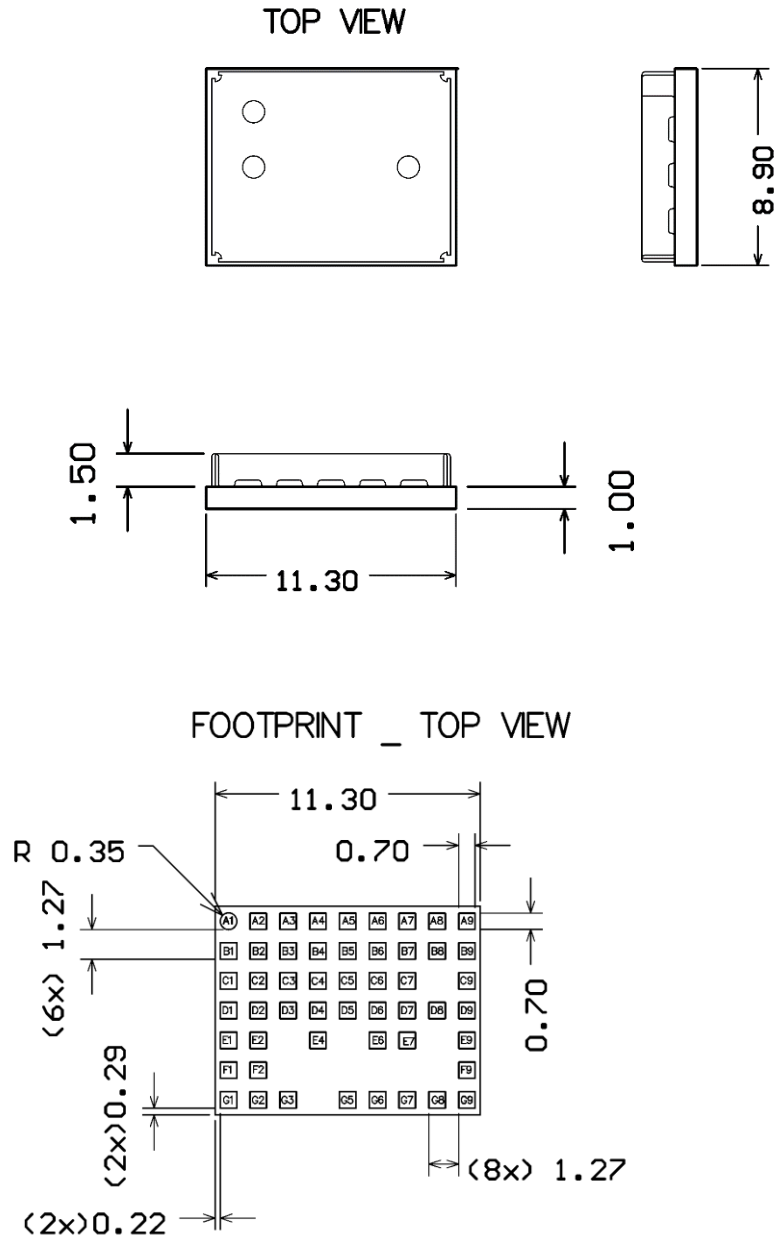
Multiple Stacks available:

- ✓ LoRaWAN™ specifications 1.0.4 (32001505BEU)
- ✓ LoRa Mipot (32001505CEU)
- ✓ LoRa Modem (32001505DEU)
- ✓ LoRa Multistack (32001505FEU)

Regulatory compliance:

- ✓ 2014/53/EU (RED)
- ✓ EN 300 220-1 v3.1.1 (2017-02)
- ✓ EN 300 220-2 v3.1.1 (2017-02)
- ✓ EN 301 489-1 v2.2.3 (2019-11)
- ✓ EN 301 489-3 v2.2.0 (2021-11)
- ✓ EN IEC 62311:2020
- ✓ IEC 62321:2008 / IEC 62321-1:2013 / IEC 62321-2:2013 / IEC 62321-3-1:2014
- ✓ EN 62321:2009/ EN 62321-1:2013 / EN 62321-2:2014 / EN 62321-3-1:2014
- ✓ UNE EN 62321:2009 / UNE EN 62321-1:2009 / UNE EN 62321-2:2014 / UNE EN 62321-3-1:2014
- ✓ EN 62368-1:2014 + AC:2015 + AC:2017 + A11:2017
- ✓ IEC 62368-1:2014 + COR1:2015 + COR2:2015
- ✓ UNE-EN 62368-1:2014 + AC1:2015 + AC2:2015 + AC:2017 + A11:2017

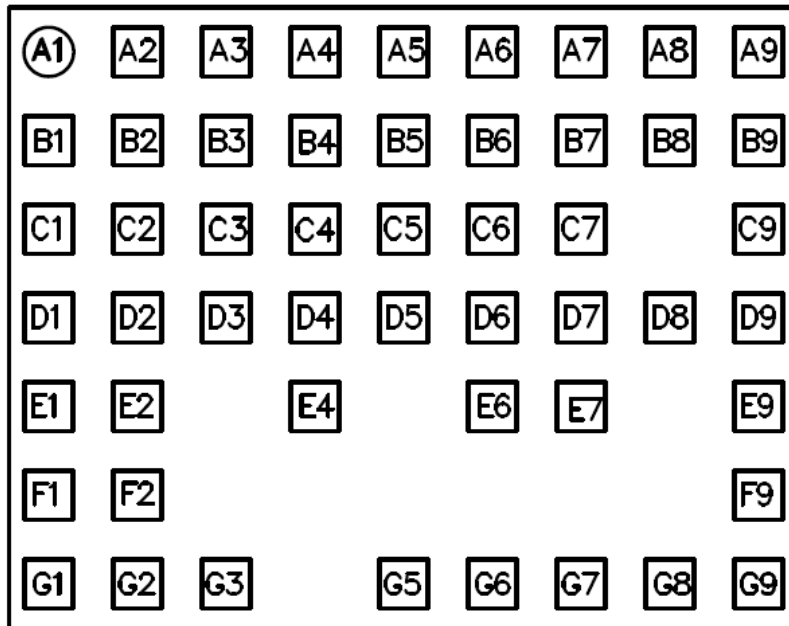
2. Mechanical Dimensions



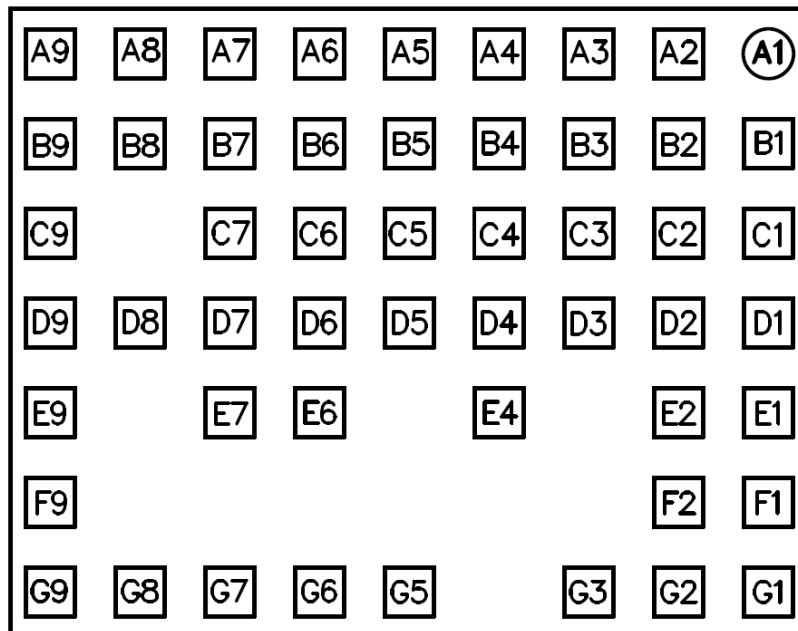
Note: Dimension in mm. General tolerance $\pm 0.1\text{mm}$. The tolerance is not cumulative

3. Pin Definition

Top View



Bottom View



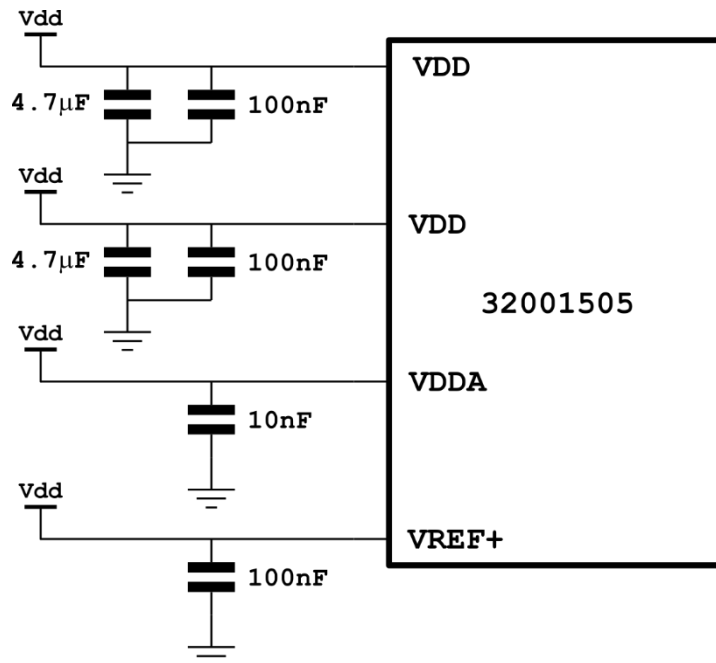
Pad	Name	Type	Pad	Name	Type
A1	SPI1_MISO	I/O	D1	GND	S
A2	SPI1_SCK	I/O	D2	NC	-
A3	SPI1_NSS	I/O	D3	NC	-
A4	LPUART1_TX	I/O	D4	GND	S
A5	LPUART1_RX	I/O	D5	NC	-
A6	SPI1_MOSI	I/O	D6	NC	-
A7	I2C1_SCL	I/O	D7	VBAT	S
A8	I2C1_SDA	I/O	D8	NC	-
A9	VDD	S	D9	SPI2_MISO	I/O
B1	NWAKE	I	E1	GND	S
B2	NDATA_INDICATE	O	E2	GND	S
B3	USART2_TX	I/O	E4	NC	-
B4	USART2_RX	I/O	E6	NC	-
B5	USART1_TX	I/O	E7	NC	-
B6	USART1_RX	I/O	E9	SPI2_MOSI	I/O
B7	NC	-	F1	ANT	RF I/O
B8	VDDA	S	F2	GND	S
B9	VDD	S	F9	SPI2_NSS	I/O
C1	BOOT0	I/O	G1	GND	S
C2	NC	-	G2	GND	S
C3	NC	-	G3	GND	S
C4	GND	S	G5	NRST	I
C5	NC	-	G6	NC	-
C6	NC	-	G7	NC	-
C7	VREF+	S	G8	NC	-
C9	GND	S	G9	SPI2_SCK	I/O

Note: NC means “do not connect”, leave the pin floating.

4. Hardware Integration

4.1. Decoupling capacitors

Each power supply pin must be decoupled with capacitors with the values suggested in the figure.



4.2. Layout guidelines

For better noise rejection, put the decoupling capacitors as close as possible to the power pins of the module, giving precedence to the low value ones.

The trace connecting to the RF pin must have an impedance of 50 Ω. For better performance, connect the GND pads around the RF pin without thermals.

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Parameter	Max.	Unit
Supply Voltage (VDD)	+3.9	V
Radio Frequency Input Level, pin F1	0	dBm
Voltage Standing Wave Ratio (VSWR) at RF Input, ANT, pin F1	10:1	
I/O Pin voltage	VDD + 0.3	V
Storage Temperature	-40 ÷ +100	°C
Operating Temperature	-40 ÷ +85	°C

6. Operating Condition

Note: All RF parameters measured with input (pad F1, ANT) connected to a 50 Ω impedance signal source or load.

GENERAL ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
Supply Voltage (VDD)	+2.1	+3.0	+3.6	V	
VDDA	0	-	+3.6	V	
VBAT	+1.55	-	+3.6	V	
VIN	-0.3	-	VDD + 0.3	V	
Sleep DC Current	-	2.2	3.0	μ A	

RECEIVER ELECTRICAL CHARACTERISTICS @ 25 °C

Parameter	Min.	Typ.	Max.	Unit	Notes
DC Current Drain	-	-	11	mA	6
Operating Frequency	868.1	-	869.525	MHz	
Channel Frequency Precision	-	\pm 15	-	kHz	
Sensitivity, 2-FSK	-	-115	-	dBm	2,3,5
Sensitivity, LoRa [®]	-	-135	-	dBm	2,4,5
Image Frequency Rejection	-	54	-	dB	7
Spurious radiated level	-	-	-57	dBm	
Output Logic Low	GND	-	0.05	V	
Output Logic High	VDD - 0.2	-	VDD	V	

TRANSMITTER ELECTRICAL CHARACTERISTICS @ 25 °C

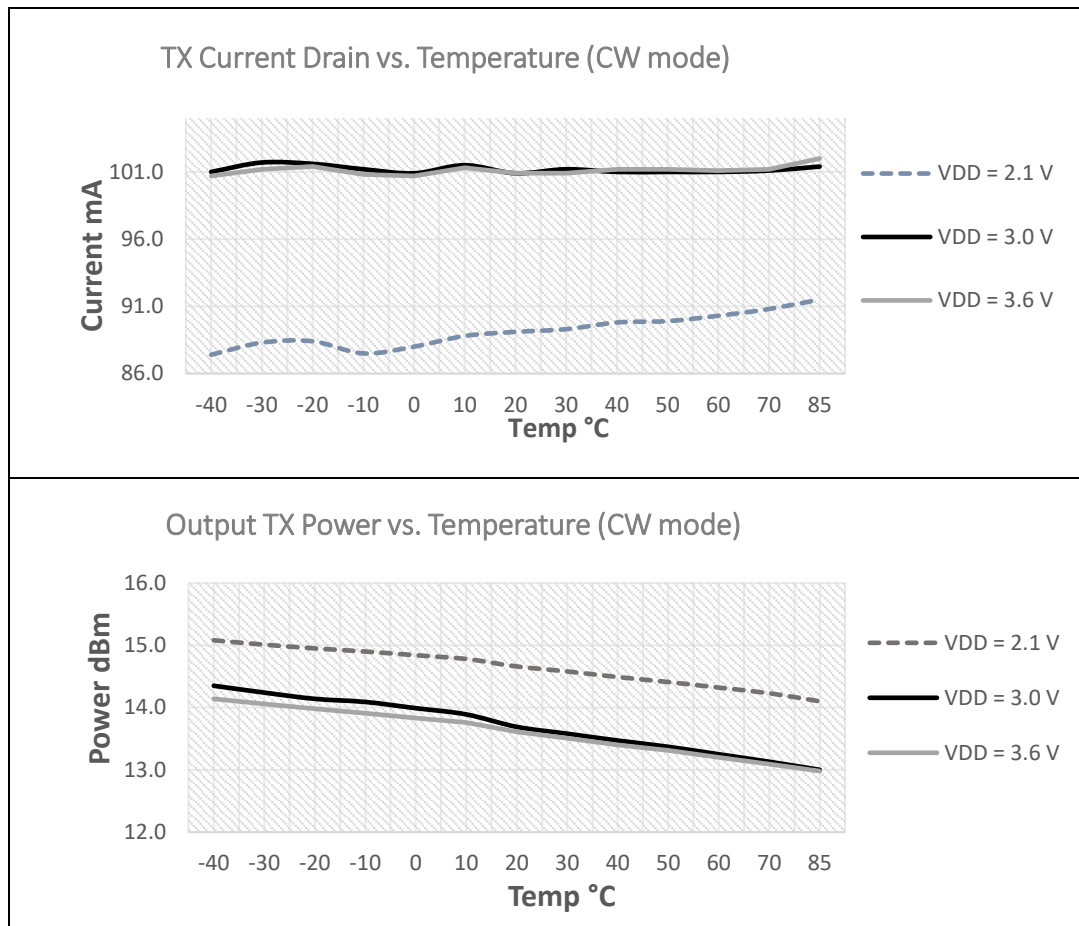
Parameter	Min.	Typ.	Max.	Unit	Notes
Current Drain (CW @14dBm)	-	103	-	mA	1,2
Operating frequency	868.0	-	868.6	MHz	
Occupied Bandwidth 2-FSK	-	125	-	kHz	
Occupied Bandwidth LoRa®	125		250	kHz	
Operating Channel Width 2-FSK	-	200	-	kHz	
Operating Channel Width LoRa®	200	-	300	kHz	
Maximum Output power (50 Ω load)	-	14	-	dBm	1,2,8
RF Output Impedance	-	50	-	Ω	
Input Logic Low	GND	-	0.05	V	
Input Logic High	VDD - 0.2	-	VDD	V	

Notes:

- 1) VDD = 3.6 V.
- 2) All RF parameters measured with input (pin F1, ANT) connected to 50 Ω impedance signal source or load.
- 3) Pseudo random code NRZ, 2-FSK BER (bit error rate) = 0.1 % or better, 2-level FSK modulation without pre-filtering, Bit Rate = 4.8 kbit/s, frequency deviation = 5 kHz, filter bandwidth = 20 kHz.
- 4) LoRa® PER (packet error rate) = 1 %, packet of 64 bytes, preamble of 8 bytes, error correction code CR = 4/5, CRC on payload enabled, no reduced encoding, no implicit header.
- 5) Sensitivities given using highest LNA gain step.
- 6) Power consumption measured with -140 dBm signal and AGC ON.
- 7) Blocking immunity, ACR and co-channel rejection, given for a single tone interferer and referenced to sensitivity +6 dB, blocking tests performed with unmodulated signal measured as per ETSI 300 220-1.
- 8) In order to not exceed the maximum power permitted by the ETSI EN 300 220 regulation, choose an appropriate antenna system and power supply.

7. Temperature Range Curves

Note: All RF parameters measured with input (pad F1) connected to a 50 Ω impedance signal source or load.



8. Safety note

To meet safety requirements, the module must be powered by an external power source that meets limits of ES1 and PS1 according to IEC 62368-1.

9. Application Notes

Title	Description	Doc
Command Reference Manual	Description of commands for the LoRaWAN stack	32001505BEU_Com_Ref
Command Reference Manual	Description of commands for the LoRa Mipot stack	32001505CEU_Com_Ref
Command Reference Manual	Description of commands for the LoRa Modem stack	32001505DEU_Com_Ref
Command Reference Manual	Description of commands for the multi-stack module	32001505FEU_Com_Ref
Manufacturing Process Information for LGA MiP Series Modules	Packaging information, Tape & Reel Specification, Reflow soldering information	AN_MNF002

10. Ordering Information

Title	Description	DoC
32001505BEU	MiP-Lw-1C128N-EU	Europe
32001505CEU	MiP-LoMi-1C128N-EU	Europe
32001505DEU	MiP-LoMo-1C128N-EU	Europe
32001505FEU	MiP-LwMo-1C128N-EU	Europe

11. Regulatory Approvals

Doc	Title	Description
DoC	32001505BEU_DoC	Declaration of Conformity

12. Revision History

Revision	Date	Description
0.0	27.05.2022	Draft
0.9	28.02.2021	Preliminary
0.10	28.04.2021	<ul style="list-style-type: none"> - Pin C4 is GND, Pin C3 is TIM2_CH2 - Added pin D4 (GND) - Bottom view of the pinout - Added TX OBW and TX OCW
0.11	08.09.2021	<ul style="list-style-type: none"> - Corrected “power down current” to “sleep current” in Product Features - V_{DD} min set to 2.1 V
1.0	11.11.2021	<ul style="list-style-type: none"> - Corrected temperature curves parameter according to V_{DD} min. - Added Top view
1.1	21.12.2021	Corrected OCW
1.2	01.02.2022	Added Safety note paragraph
1.3	01.06.2022	<ul style="list-style-type: none"> - Template change - Add NWAKE, NDATA_INDICATE and NRST signals in the pin description
1.4	28/09/2022	- Change to family datasheet