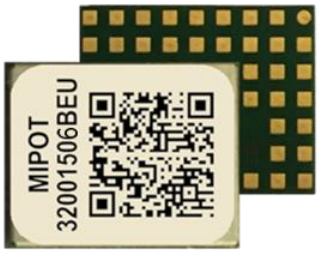
Wireless Protocol Modules MiP Series 32001506xxx

Communication Interface



Description

This document presents connection methodologies for communicating with family modules 32001506xxx.

The 32001506xxx family is based on STM32WL55 dual core Arm® Cortex-M4/Cortex-M0+ microcontroller.

Contents

1. Communication interface

The **32001506xxx** is a module where the core Arm Cortex-M0+ is used exclusively for radio management and radio protocol implementation while the core Arm Cortex-M4 is fully available for user application. In this scenario the Arm Cortex-M4 configures and operates the radio part controlled by the Arm Cortex-M0+. The communication interface between cores is the STM32WL55's internal block named Inter-Processor Communication Controller (IPCC).

1.1. IPCC – Inter-Processor Communication Controller

IPCC is an ST Microcontroller proprietary inter-core communication controller. For details please refer to "*RM0453 Reference manual - STM32WL5x advanced Arm®-based 32-bit MCUs with sub-GHz radio solution*".

IPCC communication is based on a common RAM memory area shared between Cortex-M4 and Cortex-M0+. In 32001506xxx such area is 1 kB wide starting from address 0x20008000 to address 0x200083FF and is used for bidirectional data exchange between cores.

The communication between the Cortex-M4 and Cortex-M0+ cores is performed with the same communication protocol defined for the physical SPI/I^2C/UART channels used into 32001505xxx module and is internally managed through transmit/receive interrupts.

Protocol messages are written/read to/from IPCC buffers located inside shared RAM area.

A simple Arm Cortex-M4 application template may be provided as basic reference to implement IPCC communication with Arm Cortex-M0+ core.

2. Revision History

Revision	Date	Description
0.1	05.12.2024	First version